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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/683,759 | 10/09/2003 | Andrew Ott | 42P17277 | 5056 |

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Michael A. Bernadicou
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025

| EXAMINER | |
|---|---|
| GOUDREAU, GEORGE A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 1763 | |

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| *Office Action Summary* | **Application No.** | **Applicant(s)** | |
|---|---|---|---|
| | 10/683,759 | OTT ET AL. | |
| | **Examiner** | **Art Unit** | |
| | George A. Goudreau | 1763 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on 02 August 2005.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 18,19 and 24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 18,19 and 24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

George A Goudreau
**GEORGE GOUDREAU**
**PRIMARY EXAMINER**
10-05

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 18-19, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong et. al. (6,485,815).

Jeong et. al. disclose two different embodiments for fabricating a device.

The first embodiment is comprised of the following steps:

-A conductive wiring pattern (110) is formed onto the surface of a wafer (100).;

-A CVD SiO2 layer (120) is optionally formed as a cap layer onto the surface of the wafer.;

-A first insulating layer (130), which is comprised of a layer of any of MSQ or SiOC, which has methyl groups on its surface, is formed onto the surface of the wafer.;

-The surface of the first insulating layer is treated with a plasma to form a adhesive layer (130 a) by removing the methyl groups from the surface of the first insulating layer up to a depth of 500 angstroms.;

-A second insulating layer or ILD (140) which is comprised of any of SiC, SiON, TEOS oxide, HDP oxide, or HSQ is formed onto the surface of the adhesive layer.;

-A via hole or dual damascene hole (h 1) is etched into the first, and second insulating layers until contact is made with the wiring layer (110).;

-A Ti-TiN barrier layer (152) is conformably formed onto the surface of the wafer.;

-An conductive layer (154) is used to form the via or dual damascene.; and

-An Al upper wiring layer (160) is formed onto the surface of the via or the Cu damascene.

In this instance layers 100, 120, 130 may be considered to be the substrate, which is claimed by the applicant. Further, the intermediate layer, and the ILD layer which are claimed by the applicant may be considered to be the same layer (i.e.-layer 140) in this process.

The second embodiment is comprised of the following steps:

-A conductive wiring pattern (210) is formed onto the surface of a wafer (200).;

-A CVD SiO2 layer (220) is optionally formed as a cap layer onto the surface of the wafer.;

-A first insulating layer (230), which is comprised of a layer of any of MSQ or SiOC, which has methyl groups on its surface, is formed onto the surface of the wafer.;

-An adhesive, buffer layer (235) which is comprised of USG (i.e.-O3-TEOS oxide) is formed onto the surface of the wafer. In the process of depositing the adhesive buffer layer onto the surface of the first insulating layer, methyl groups are removed from the surface of the first insulating layer.;

-A second insulating layer or ILD (240) which is comprised of any of SiC, SiON, TEOS oxide, HDP oxide, or HSQ is formed onto the surface of the buffer layer.;

-A via hole or dual damascene hole (h 2) is etched into the first, and second insulating layers until contact is made with the wiring layer (210).;

-A Ti-TiN barrier layer (252) is conformably formed onto the surface of the wafer.;

-An conductive layer (254) is used to form the via or dual damascene.; and

-An Al upper wiring layer (260) is formed onto the surface of the via hole or the Cu damascene.

In this instance layers 200, 220, 230 may be considered to be the substrate which is claimed by the applicant. Further, the intermediate layer which is claimed by the applicant is layer (235). The ILD layer which a claimed by the applicant is layer (240). This is discussed specifically in columns 4-10; and discussed in general in columns 1-14. This is shown in figures 1-11. Jeong et. al. fail, however, to specifically disclose the following aspects of applicant's claimed invention:

-the formation of a graded region of the substrate to the specific depths which are claimed by the applicant; and

-the electrical connection of a package to the wiring layer (i.e.-connector) in the device formed above

It would have been obvious to one skilled in the art to form the graded region or buffer layer in the devices which are taught above to the specific thickness which are claimed by the applicant based upon the following. It would have been desirable to form an adhesive layer, which is sufficiently thick to provide adequate adhesion between the two insulating layers such that delamination does not occur during subsequent cmp step between these two insulating layers without undesirably providing an excessively thick adhesive layer, which would waste precious processing time, and processing money.

It would have been obvious to one skilled in the art to electrically connect a package to the second wiring layer in the device fabricated above based upon the following. It is conventional or at least well known in the semiconductor processing arts to electrically connect a package to a wiring layer on a device in order to fabricate an electrical device. (The examiner takes official notice in this regard.) Further, the device, which is fabricated above, is obviously being provided with means for electrically connecting the wafer to another device such as a package.

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5. Applicant's arguments with respect to claims of record have been considered but are moot in view of the new ground(s) of rejection.

6. This action will not be made final due to the new grounds of rejection.

7. Any inquiry concerning this communication should be directed to examiner George A. Goudreau at telephone number (571)-272-1434.

George A Goudreau

George A. Goudreau
Primary Examiner
Art Unit 1763